Evaluation Board for the AD9834 Direct Digital Synthesizer

EVAL-AD9834EB

FEATURES

Full-featured evaluation board for the AD9834
Various linking options
PC software for control of AD9834
On-board patchwork area

INTRODUCTION

This data sheet describes the evaluation board for the AD9834 direct digital synthesizer (DDS). The AD9834 is a numerically controlled oscillator using a phase accumulator, a sine look-up table, and a 10-bit DAC. The AD9834 can be operated with clock frequencies up to 75 MHz. Both phase modulation and frequency modulation can be performed with the AD9834. Complete specifications for the AD9834 are available in the AD9834 data sheet and should be consulted in conjunction with this data sheet when using the evaluation board.

The evaluation board interfaces to the parallel port of a PC. Software is available with the evaluation board that allows the user to easily program the AD9834.

The AD9834 evaluation board includes a 75 MHz oscillator that provides the MCLK for the AD9834. The user can remove this oscillator, if required, and drive the AD9834 with a different clock oscillator or an external clock source via a BNC connector. A digital buffer is also on the board so that the signals from the edge connector are buffered.

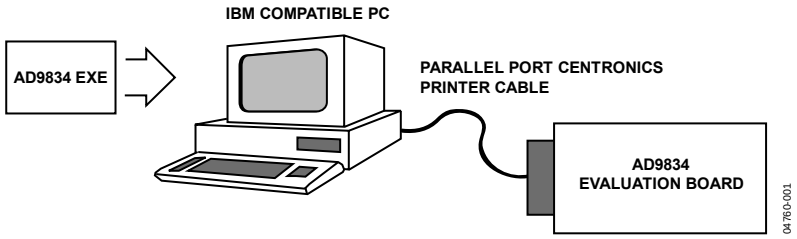

Figure 1. Evaluation Board Setup

Rev. A

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REVISION HISTORY

12/06—Rev. 0 to Rev. A

Changes to Format ..... Universal
Changes to Introduction 1
Changes to Power Supplies Section and LK3 Section 3
Changes to Table 10 9

6/04—Revision 0: Initial Version

HARDWARE DESCRIPTION

POWER SUPPLIES

This evaluation board has two analog power supply inputs: AVDD (Analog V_{DD}) and AGND (Analog GND). There are also two digital supplies on the part, DVDD (Digital V_{DD}) and DGND (Digital GND). Both of these supplies are independent of each other, and can be powered from 2.3 V to 5.5 V.

As well as supplying the digital supply for the AD9834, DVDD is used to provide the supply for the 75 MHz oscillator and the digital buffer.

DGND and AGND are connected under the AD9834; therefore, it is recommended not to connect AGND and DGND elsewhere in the system. All power supplies are decoupled to the relevant ground plane using 10 µF tantalum capacitors and 0.1 µF ceramic capacitors at the input to the evaluation board. The power supplies are again decoupled using 0.1 µF capacitors at the AD9834, the crystal, and the logic.

LINK AND SWITCH OPTIONS

The five link options (LK1, LK2, LK3, LK4, and LK5) must be set before using the evaluation board.

LK1

If the programming method selected is hardware (that is, a standalone board), LK1 operates as follows:

- With LK1 in Position A, PSEL can be controlled from an external logic source through the SMB connector, PSEL1.
- With LK1 in Position B, PSEL is connected to SW1, allowing the user to control the PSEL signal using the double throw switch, SW1-2.

If the programming method selected is software (that is, board controlled through a PC), LK1 is ignored.

LK2

If the programming method selected is hardware, LK2 operates as follows:

- With LK2 in Position A, FSEL can be controlled from an external logic source through the SMB connector, FSEL1.
- With LK2 in Position B, FSEL is connected to SW1, allowing the user to control the FSEL signal using the double throw switch, SW1-3.

If the programming method selected is software, LK2 is ignored.

LK3

The AD9834 evaluation board contains an on-board 75 MHz oscillator that provides the MCLK for the AD9834.

When LK3 is open, the on-board oscillator is used.

If the user requires the AD9834 to be driven from an external clock source via the SMB connector, CLK1, the on-board 75 MHz oscillator must be removed from the board, and LK3 is closed.

LK4

The digital section of the AD9834 is driven by an on-chip regulator that steps down the applied DVDD voltage to 2.5 V when DVDD exceeds 2.5 V.

If the user applies a voltage greater than 2.5 V to the input DVDD, LK4 should be opened.

If the user applies a voltage of 2.5 V to DVDD, the regulator can be bypassed by closing LK4.

Note that the components on the evaluation board and the Centronics connector do not operate at 2.5 V. For evaluation of the AD9834 at 2.5 V, the evaluation board should be used as a standalone board, with the user supplying the SCLK, SDATA, FSYNC, and RESET externally. The digital buffer and the oscillator should also be replaced with 2.5 V compatible devices.

LK5

The AD9834 has a SLEEP pin that allows sections of the device that are not being used to be powered down to minimize the current consumption.

With LK5 in Position B, the AD9834 is fully powered up, and the sleep function is not being used.

With LK5 in Position A, the on-chip DAC on the AD9834 is powered down, which is useful in applications where a clock output is being generated using the MSB from the NCO.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. Table 1 shows the position in which all the links are set when the evaluation board is packaged.

Table 1. Initial Link and Switch Positions

Link No.	Initial Position	Function
LK1	B	LK1 is arranged so that PSEL is tied to SW1-2.
LK2	B	LK2 is arranged so that FSEL is tied to SW1-3.
LK3	Open	LK3 is arranged so that the on-board oscillator is used.
LK4	Open	The user is not applying a voltage of 2.5 V to DVDD.
LK5	B	LK5 is arranged so that the AD9834 is fully powered up.
SW1	DVDD	All the SW1 switches are arranged so that DVDD is selected.

EVALUATION BOARD INTERFACING

The evaluation board interfaces via a 36-way Centronics female connector, J1. The pinout for the J1 connector is shown in Figure 2, and its pin designations are given in Table 4.

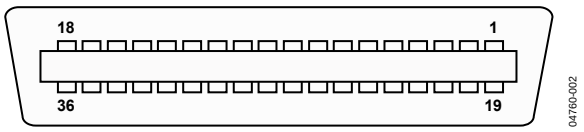

Figure 2. Pin Configuration for 36-Way Connector, J1

SOCKETS

The seven sockets relevant to the operation of the AD9834 on this evaluation board are described in Table 2.

Table 2. Socket Functions

Socket	Function
CLK1	Subminiature BNC socket for the MCLK input
FSEL1	Subminiature BNC socket for FSELECT
PSEL1	Subminiature BNC socket for PSEL
IOUT	Subminiature BNC socket for IOUT
IOUTB	Subminiature BNC socket for IOUTB
SBOUT	Subminiature BNC socket for SBOUT

CONNECTORS

The three connectors on the AD9834 evaluation board are described in Table 3.

Table 3. Connector Functions

Connector	Function
J1	36-way Centronics connector.
J2	PCB mounting terminal block. The digital power supply to the evaluation board is provided via this connector.
J3	PCB mounting terminal block. The analog power supply to the evaluation board is provided via this connector.

SWITCHES

The AD9834 evaluation board has an end-stackable switch that can be used to control the FSEL and PSEL inputs.

Table 4. 36-Way Connector Pin Functions

Pin No.	Mnemonic	Description
2	SCLK	Serial Clock. The signal on this pin is buffered before being applied to the SCLK pin of the AD9834. The AD9834 requires an external serial clock when data/control information is being written to the device. The serial clock can be continuous, or it can idle high or low between write operations.
3	SDATA	Serial Data. Data applied to this pin is buffered before being applied to the AD9834. The serial data applied to the SDATA pin is written to the serial register of the device. The data is then transferred to the destination register or the control register. The two MSBs of the 16-bit word being written are used to identify the destination for the data information. The AD9834 accepts CMOS logic levels.
4	FSYNC	The signal on this pin is buffered before being applied to the FSYNC pin of the AD9834. The FSYNC signal frames the 16-bit word being loaded into the AD9834, the signal going low for 16 SCLK cycles.
14	RESET	Active High Digital Input. RESET resets the phase accumulator to 0, which corresponds to an analog output of midscale.
19 to 30	DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board.
1, 5 to 13, 15 to 18, 31 to 36		No Connect.

SOFTWARE DESCRIPTION

The AD9834 evaluation board is shipped with a CD containing software that can be installed on any standard PC to control the AD9834. The PC is connected to the evaluation board by a standard Centronics printer cable.

SOFTWARE REQUIREMENTS

The software runs on any PC that meets the following requirements:

- Microsoft Windows® 98, Windows 2000, or Windows XP® installed
- At least 8 Mb of RAM

The software is distributed on a single CD that contains all the files required to install and run the software.

INSTALLING THE SOFTWARE

To install the software:

1. Start Windows and insert the CD.

   The installation software should launch automatically. If it does not, use Windows Explorer to locate the file **setup.exe** on the CD. Double-clicking on this file starts the installation procedure.

2. At the prompt, select the destination directory, which is C:**Program Files\Analog Devices\AD9834** by default.

   Once the directory is selected, the installation procedure copies the files into the relevant directories on the hard drive. The installation program creates a program group called **Analog Devices** with subgroup **AD9834** in the **Start** menu of the taskbar.

3. Once the installation procedure is complete, double-click the **AD9834 icon** to start the program.

EVALUATION SOFTWARE

When the program starts, it checks the PC BIOS to detect the address of the printer port installed. The three possible base addresses at which a printer port can reside are shown in Table 5.

Table 5.

Printer	Base Address (Hex)
LPT1	0x378
LPT2	0x278
PRN1	0x3BC

If more than one printer port is installed, the software chooses the first one it finds. The user can change the printer port from the **Printer Port** menu of the main window.

USING THE EVALUATION BOARD INTERFACE

Figure 3 shows the main window of the AD9834 evaluation board software when the program starts.

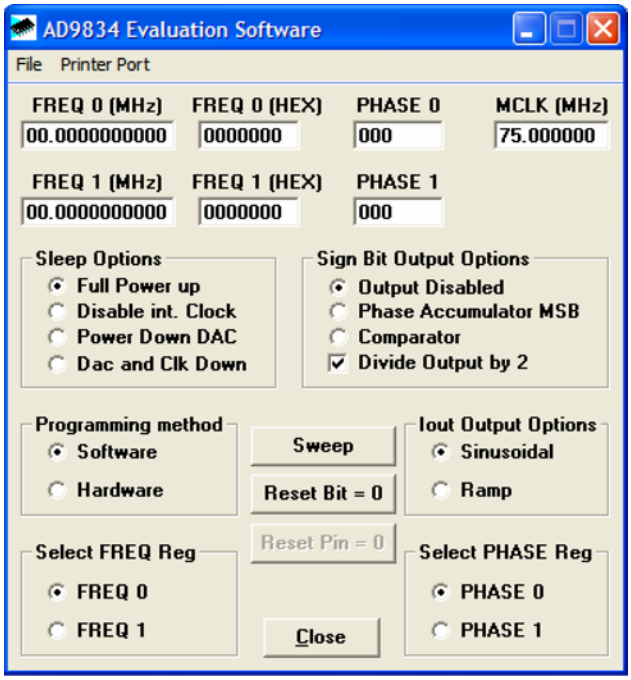

Figure 3. Main Window

From the main window, the user can control all the functionality of the AD9834. The main features are listed below and described in detail in the sections that follow.

- Access to both Frequency Register 0 and Frequency Register 1
- Access to both Phase Register 0 and Phase Register 1
- Access to the RESET bit
- Ability to sweep through a frequency range using either the Frequency Register 0 or Frequency Register 1
- Access to the programming method
- Access to the sleep options
- Access to sign bit output options
- Access to the IOUT output options

FREQUENCY REGISTERS

The AD9834 contains two frequency registers that can be programmed individually. The evaluation board software allows the user to enter any frequency value between 0 Hz and half the master clock frequency. If a value outside this range is entered, the software chooses the closest valid value. The frequency value is converted to a 28-bit decimal number that is loaded to the appropriate frequency register after clicking **Enter**. The hexadecimal equivalent is also displayed in the main window.

PHASE REGISTERS

The AD9834 contains two phase registers that can be individually loaded with different values. The phase numbers are entered as integer values between 0 and 4095 (corresponding to 0° to 360° phase shift). The values are loaded to the appropriate phase register after clicking **Enter**.

RESET MODE

The RESET bit in the control register of the AD9834 is controlled by the **Reset Bit = 0** and **Reset Bit = 1** buttons of the AD9834 evaluation board software. The RESET bit is initialized to 0 on power-up by the AD9834 evaluation software. Setting the RESET bit to 1 (by clicking **Reset Bit = 1** in the main window) sets the phase accumulator to zero phase corresponding to an analog output of midscale.

SWEEP FACILITY

Clicking **Sweep** in the main window displays the **Sweep Output Frequency** dialog box, which can be used to program the AD9834 to produce a continuously increasing or decreasing frequency sweep. The user can enter a start frequency, a stop frequency, or a step frequency. There is also the option of setting the delay between steps, and the number of time the sweep is to be repeated.

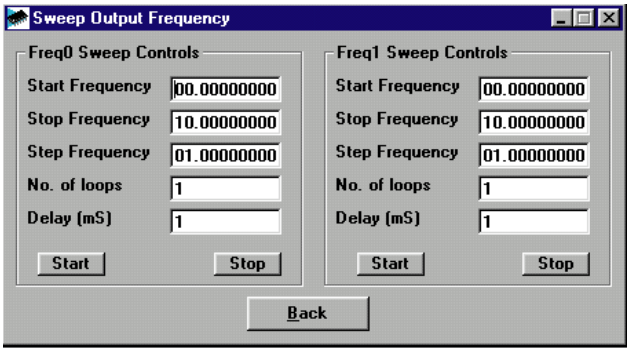

Figure 4. Sweep Dialog Box

The sweep values in the following example generate the frequency outputs shown in Table 6. If the frequency span is not an integer multiple of the step frequency, the span from the second to last frequency to the last frequency is such that the stop frequency is the last frequency output to the AD9834.

Table 6. Sweep Value Example

Start Frequency (MHz)	**1.00000**
Stop Frequency (MHz)	1.70000
Step Frequency (MHz)	0.20000
Frequency Outputs (MHz)	1.00000
	1.20000
	1.40000
	1.60000
	1.70000

Both Frequency Register 0 and Frequency Register 1 can be loaded with separate frequency, step, delay, and loop information, but the output from the AD9834 depends on which frequency register is selected via the FSEL pin or Freq Reg bit.

PROGRAMMING METHOD

The choice of programming method controls the selection of the frequency and phase registers used to provide the output. If the hardware option is chosen, the frequency and phase selection come from the FSEL and PSEL pins, respectively. This disables changing the frequency and phase registers from software as required. If the software option is chosen, the registers are selected by software. Note that registers are not set to a known value on power-up, so the user should set all the registers to a known value.

SLEEP OPTIONS

The control register of the AD9834 contains two sleep bits that put the part into a power-down mode. The sleep options on the evaluation board provide full access to both bits (see Table 7).

Table 7. Sleep Options

Option	Description
Full Power-Up	Nothing on the AD9834 chip is powered down.
Disable Internal Clock	The internal clock of the AD9834 is disabled. The DAC output remains at its present value as the NCO is no longer accumulating.
Power-Down DAC	The DAC on the AD9834 is powered down. This is useful when the AD9834 is used to output the NCOs MSB only. Note that this option corresponds to the SLEEP pin. When the chosen programming method is hardware, this option is ignored as the SLEEP pin controls the power-up/-down operation of the DAC.
DAC and CLK Down	Both the CLK and the DAC are powered down.

SIGN BIT OUTPUT OPTIONS

The sign bit output options control what the user sees on the SIGN BIT OUT pin. The options are described in Table 8. The user can access this pin through the SMB SBOUT.

Table 8. Sign Bit Output Options

Option	Description
Output Disabled	There is no output at SIGN BIT OUT.
Phase Accumulator MSB	The MSB from the phase accumulator is connected to the SIGN BIT OUT pin.
Comparator	This connects the on-chip comparator of the AD9834 to the SIGN BIT OUT pin.
Divide Output by 2	This determines the frequency of the square waveform on the SIGN BIT OUT pin. The user has the option to divide this frequency by 2 by checking this box.

IOUT OUTPUT OPTIONS

The AD9834 provides two IOUT output options (see Table 9).

Table 9. IOUT Output Options

Option	Description
Sinusoidal	The output from the SIN ROM is fed to the DAC, which results in a sinusoidal output in IOUT.
Ramp	The SIN ROM can be bypassed so that a linear up/down ramp is output from the DAC.

ADDITIONAL INFORMATION

For more information about the current version of software and the system, go to the **File/About** menu of the main window.

EVALUATION BOARD SCHEMATIC AND ARTWORK

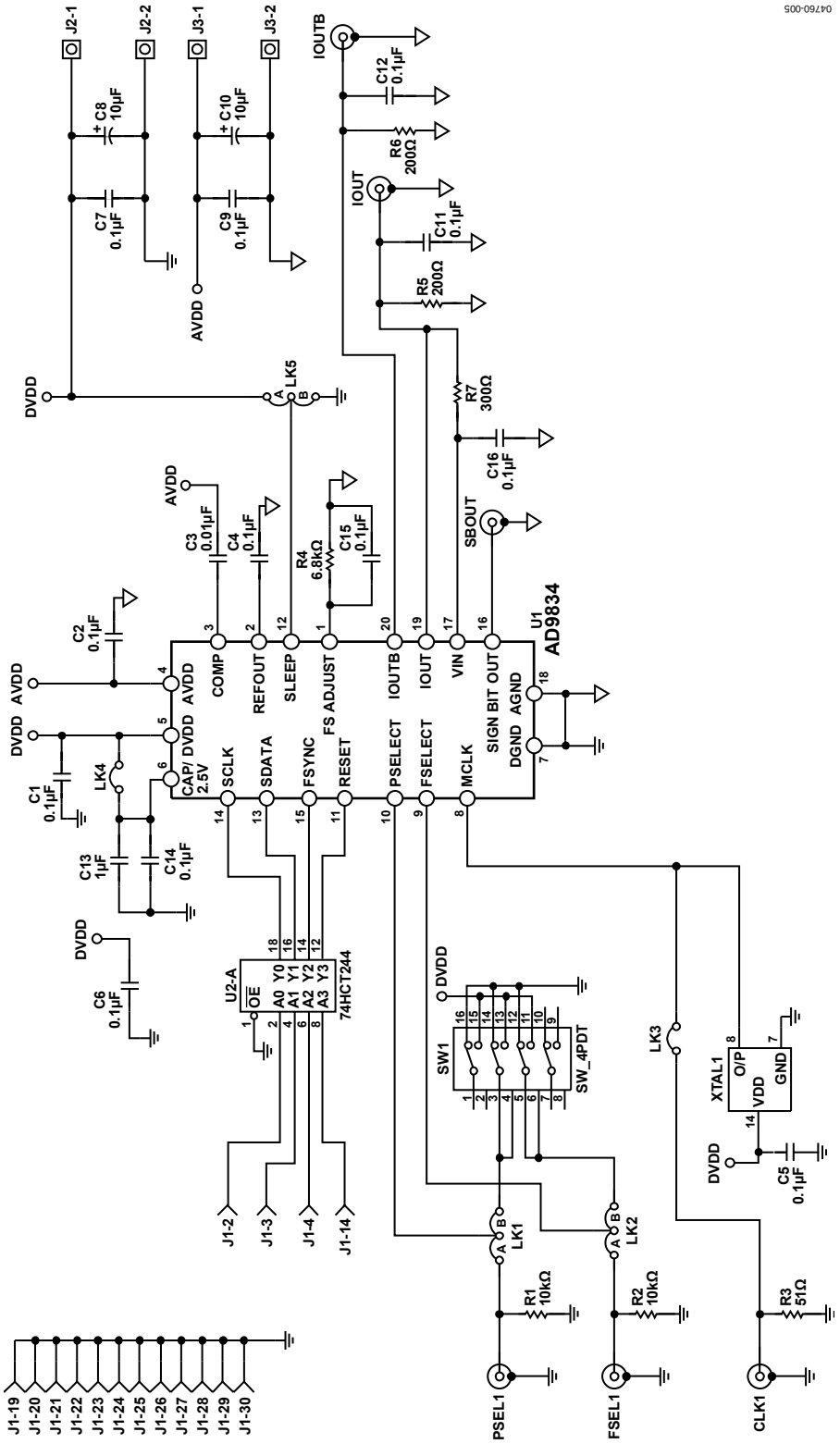

Figure 5. EVAL-AD9834EB Schematic

COMPONENT LISTING

Table 10.

Qty	Reference Designation	Device	Description	Manufacturer	Part No.
1	U1	IC	AD9834CRUZ	Analog Devices, Inc.	AD9834CRUZ
1	U2	IC	74HCT244 -	Farnell	FEC 382-267
1	SW1	Switch	Double throw, end-stackable switch	Farnell	FEC 422-708
1	XTAL1	Crystal	75 MHz CMOS/TTL crystal	AEL	AEL O75M000000L001
8	C1, C2, C4, C5, C6, C7, C9, C14	Capacitors	0.1 µF ceramic capacitor	Farnell	FEC 3549641
1	C3	Capacitor	0.01 µF ceramic capacitor	Farnell	FEC 3549616
2	C8, C10	Capacitors	10 µF tantalum capacitor	Farnell	FEC 9708340
4	C11, C12, C15, C16	Capacitors	Option for extra capacitors		Not Inserted
1	C13	Capacitor	1 µF ceramic capacitor	Digi-Key	495-1077-1-ND
2	R1, R2	Resistors	10 kΩ resistor	Farnell	FEC 9341110
1	R3	Resistor	51 Ω resistor	Farnell	FEC 9342044
1	R4	Resistor	6.8 kΩ resistor	Farnell	FEC 9342168
2	R5, R6	Resistors	200 Ω resistor	Farnell	FEC 9341471
1	R7	Resistor	300 Ω resistor		Not inserted
6	PSEL1, FSEL1, CLK1, IOUT, SBOUT, IOUTB	Sockets	50 Ω gold-plated, SMB jack	Farnell	FEC 4194512
1	J1	Connector	36-way Centronics connector	NorComp	112-036-213R001
3	LK1, LK2, LK5	Links	3-pin sil header	Farnell	FEC 1022248, FEC 148-029
2	LK3, LK4	Links	2-pin sil header	Farnell	FEC 1022247, FEC 148-029
34	U2, XTAL1	Sockets	Low profile sockets	Farnell	FEC 519-959
2	J2, J3	Connectors	2-way terminal block	Farnell	FEC 151-789
4	Rubber-Stick-On Feet		Each corner	Farnell	FEC 651-813

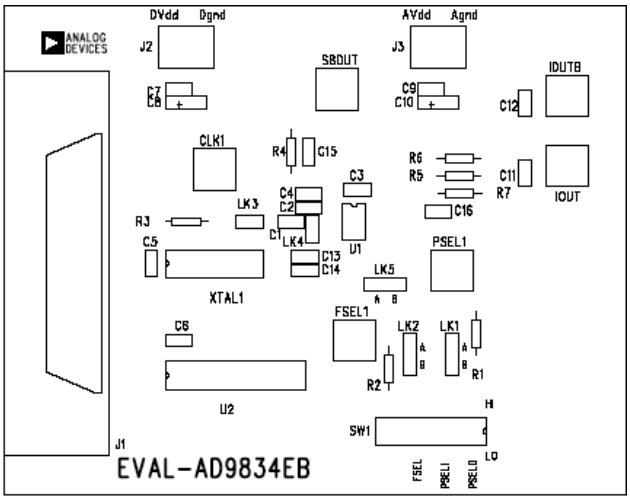

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Figure 6. EVAL-AD9834EB Silkscreen

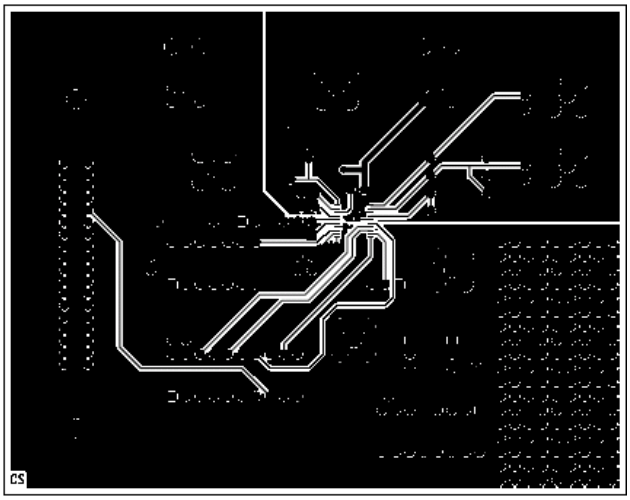

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Figure 7. EVAL-AD9834EB Component Side

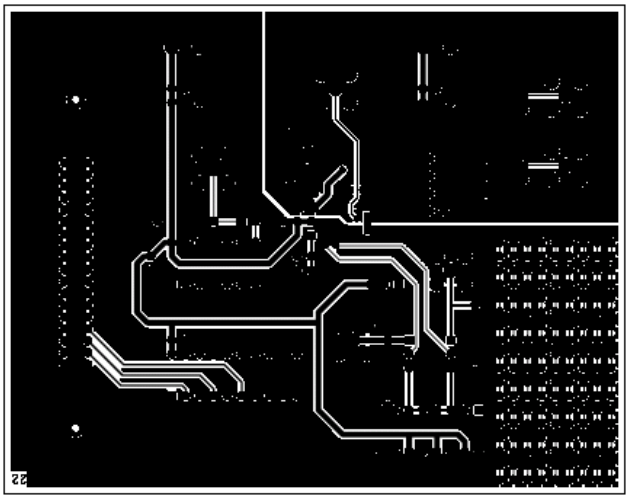

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Figure 8. EVAL-AD9834EB Solder Side

ORDERING INFORMATION

ORDERING GUIDE

Model	Description
EVAL-AD9834EB	Evaluation Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

NOTES

EB04760-0-12/06(A)